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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/875,698	06/06/2001	Sung Gyu Pyo	29936/37431	7907

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EXAMINER

UMEZ ERONINI, LYNETTE T

ART UNIT

PAPER NUMBER

1765

DATE MAILED: 04/25/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/875,698

Applicant(s)

PYO, SUNG GYU

Examiner

Lynette T. Umez-Eronini

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-11 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-11 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.  
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).  
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s) \_\_\_\_.
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 6. 6) ☐ Other:

## DETAILED ACTION

### *Information Disclosure Statement*

1. The information disclosure statement filed March 27, 2003 fails to comply with the provisions of 37 CFR 1.97, 1.98 and MPEP § 609 because Korean Patent KR-1998-065748 lacks an English translation and "Communication from Korean Intellectual Property Office dated March 13, 2003, 2 pages is missing. It has been placed in the application file, but the information referred to therein has not been considered as to the merits. Applicant is advised that the date of any re-submission of any item of information contained in this information disclosure statement or the submission of any missing element(s) will be the date of submission for purposes of determining compliance with the requirements based on the time of filing the statement, including all certification requirements for statements under 37 CFR 1.97(e). See MPEP § 609 ¶ C(1).

### *Claim Rejections - 35 USC § 103*

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

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3. Claims 1-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Li et al. (US 6,040,243) in view of Koh (US 2001/0019891 A1) and further in view of Liu et al. (US 6,177, 347).

As pertaining to claims 1-11, Li teaches, "Referring now more particularly to **FIG. 5**, there is illustrated . . . a dual damascene interconnect trench and via trench as shown. A semiconductor substrate **60** is preferably composed of monocrystalline silicon. Copper traces **68** are conventionally provided through an isolation layer **62** overlying the semiconductor substrate **60**" (column 3, lines 49-56). . . "A first dielectric layer **76** (same as applicant's first dielectric layer) is deposited . . ." (column 4, lines 5-7) . . . "An etch stopping layer **80** (same as applicant's second insulating film) is deposited overlying the first dielectric layer **76** . . ." and "the etch stopping layer **80** is typically comprised of silicon nitride" (column 4, lines 12-18). "A second dielectric layer **84** (same as applicant's third dielectric layer) is deposited overlying the etch stopping layer **80** . . ." (column 4, lines 5-25). The aforementioned reads on,

A method of forming a metal wiring in a semiconductor device, the method comprising:

providing a substrate with a lower metal layer overlying the substrate and an interlayer insulating film comprising first, second and third insulating films formed on the lower metal layer; and

forming a damascene pattern comprising a trench and a via on the interlayer insulating film, a portion of the second insulating film forming a bottom of the trench, a portion of the lower metal layer forming a bottom of the via, the trench and the via each

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comprising a sidewall.

Li further teaches, "Referring now to FIG. 6, . . . barrier layer **92** is deposited overlying . . . layer **76**, . . . layer **80**, . . . layer **84** . . . The thickness of the barrier layer **92** is between 50 Angstrom and 2000 Angstroms. . . . The barrier layer **92** may be comprised of any of the group of: metals, such as tantalum and titanium; metal nitrides, such as . . . titanium nitride, metal silicon nitrides, . . . Combinations of metals, metal nitrides, metal silicon nitrides, . . . and metal oxides can also be used for the barrier layer **92**" (column 4, lines 45-65). The aforementioned reads on.

forming diffusion prevention film spacers on the sidewalls of the trench and the via.

Li further teaches, "A copper seed layer is first deposited using . . . chemical vapor deposition (CVD). Then the copper layer **100** is the deposited by electrochemical plating" (column 5, lines 37-40), which reads on,

forming a copper layer on the diffusion prevention spacer.

Li also teaches, "The copper layer **100** is polished using conventional chemical mechanical polishing (CMP)" (column 5, lines 46-50), which reads on,

performing a chemical mechanical polishing process to form a copper metal wiring from the copper layer,

Li differs in failing to teach selectively forming chemical enhancer layers on the portion of the second insulating film forming the bottom of the trench and on the portion of the lower metal layer forming the bottom of the via; and forming a copper layer on the chemical enhancer layers by means of chemical vapor deposition method.

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Koh teaches, **FIG. 1c**, the sample (same as applicant's chemical enhancer layer) prepared as described above is treated with ethyl iodide as a catalyst **150** using a custom designed reaction chamber in 5 Torr level of vacuum. Subsequently, the silicon substrate sample is treated for about 3 minutes with a copper source material (hfac)Cu(vtms), where the ligand (hfac) means (hexafluoroacetylacetonate) and the ligand (vtms) means (Vinyltrimethylsilane), at 180°C and under 0.7 Torr of partial pressure of the copper source material (hfac)Cu(vtms) out of the total pressure of 5 Torr with argon carrier gas, to fill the holes with copper **160** as shown in **FIG. 1d**, . . ."

[0045]. "The catalyst ethyl-iodide is also applied as shown in **FIG. 1c** to form an additional copper layer **260** by means of a copper CVD using catalyst, whereby the second copper layer **260** is made thick enough (no more than 100 nm) to be used as an electrode for electroplating on top of the copper layer **260**. Completely-filled copper layer **270** by means of electroplating is shown in **FIG. 2b**." [0052]. "Referring to **FIG. 3a**, conducting layer **342** is . . . on top of a substrate **300** . . . Next, in reference to **FIG. 3b** in order to fill a contact hole **322** and trench **324**, a copper seed layer **344** is formed using a copper CVD method using ethyl-iodide ( $\text{CH}_3\text{CH}_2\text{I}$ ) as a catalyst after covering the entire surface with a barrier layer **302** that prevents conducting material from penetrating into the insulating layer during subsequent processing steps ([0055]). Since Koh uses the same material in forming chemical enhancer layers, which lines a barrier layer, which overlies a trench and via, as that of the claimed invention, then using Koh's method of forming a conductive layer would result in selectively forming chemical enhancer layers on the portion of the second insulating film forming the bottom of the

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trench and on the portion of the lower metal layer forming the bottom of the via; and forming a copper layer on the chemical enhancer layers by means of chemical vapor deposition method.

It is the examiner's position that it would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Li by using Koh's method of forming chemical enhancer layer for the purpose of "... filling deep via holes small in diameter by means of copper CVD using catalyst, where conventional methods such as electroplating process cannot be used for such small geometries ... " (Koh, [0036]).

Li in view of Koh differ in failing to teach performing a hydrogen reduction annealing, **in claim 1**.

Liu teaches, "A reactive plasma cleaning step is used to reduce copper oxide to copper and thus remove the copper oxide ... For example, H<sub>2</sub>/He plasma ... can be used. ... and "when using H<sub>2</sub>/He plasma, ... temperature of between about 25 and 300°C ... " (column 5, lines 7-18), which reads on, performing a hydrogen reduction annealing.

It is the examiner's position that it would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Li in view of Koh by using Liu's method of performing a hydrogen reduction annealing for the purpose of removing polymer buildup and copper oxide before deposition of the barrier layer underlying the subsequent metallization (Liu, column 5, lines 44-48).

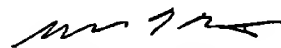
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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lynette T. Umez-Eronini whose telephone number is 703-306-9074. The examiner is normally unavailable on the First Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Benjamin Utech can be reached on 703-308-3836. The fax phone numbers for the organization where this application or proceeding is assigned are 703-972-9310 for regular communications and 703-972-9311 for After Final communications.

ltue

April 21, 2003

  
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